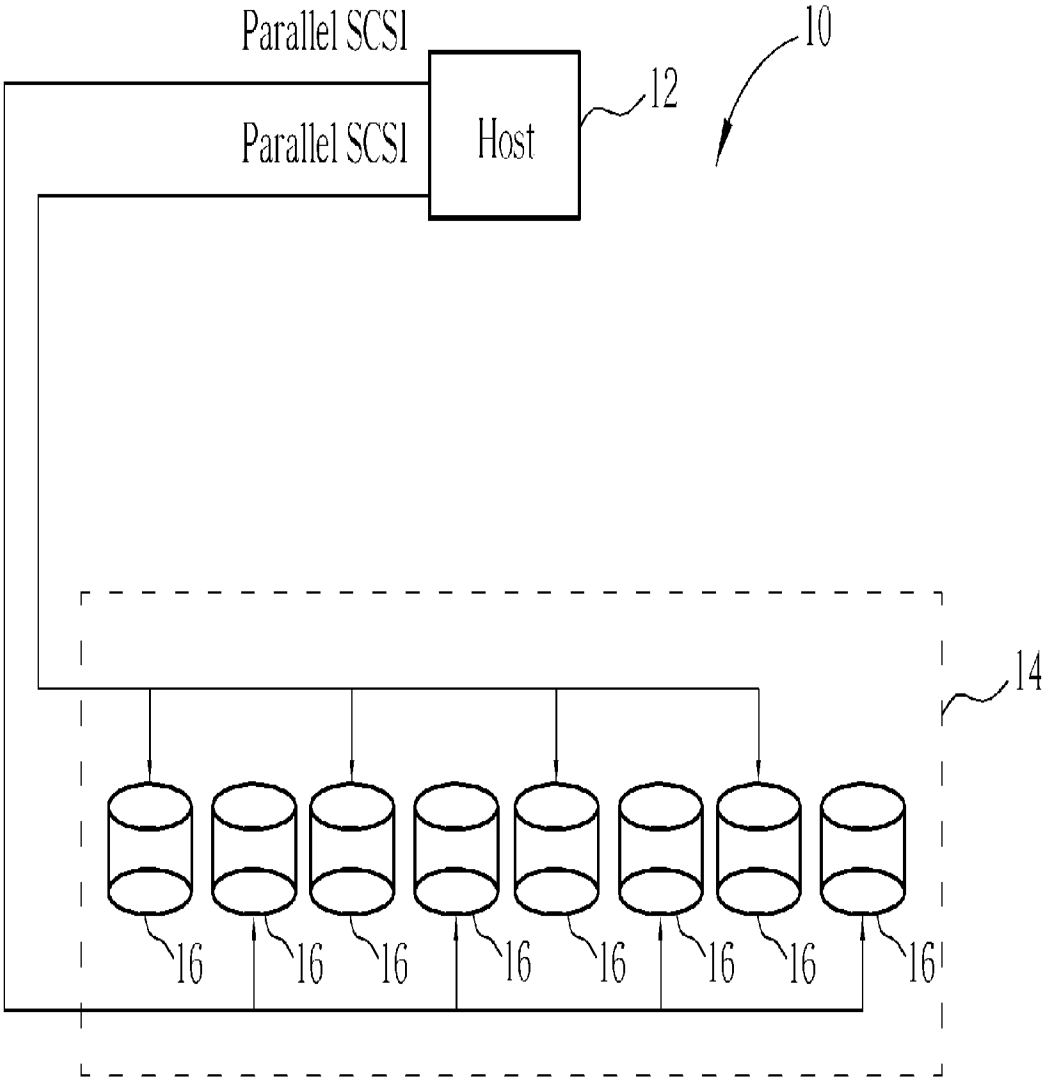

Fig. 1 Prior Art

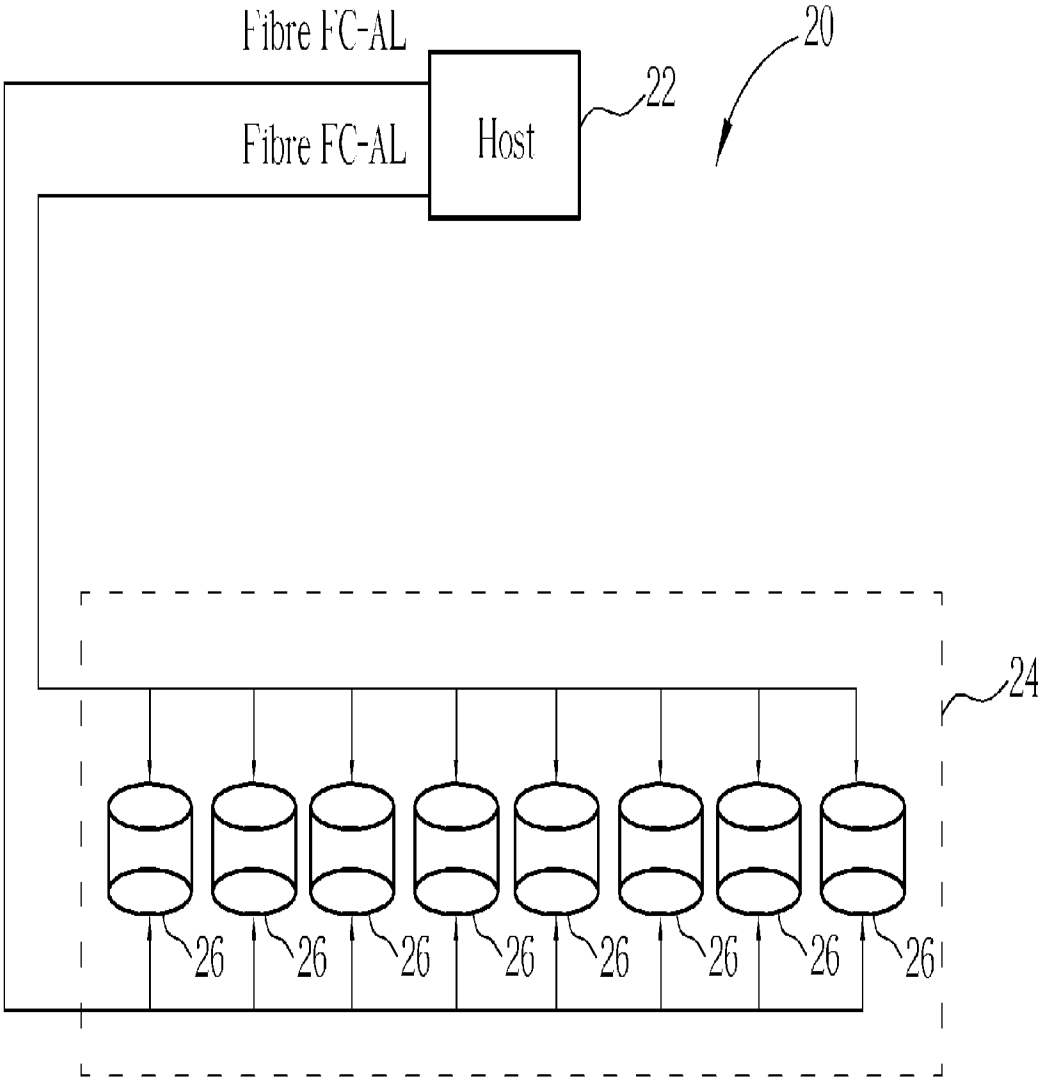

Fig. 2 Prior Art

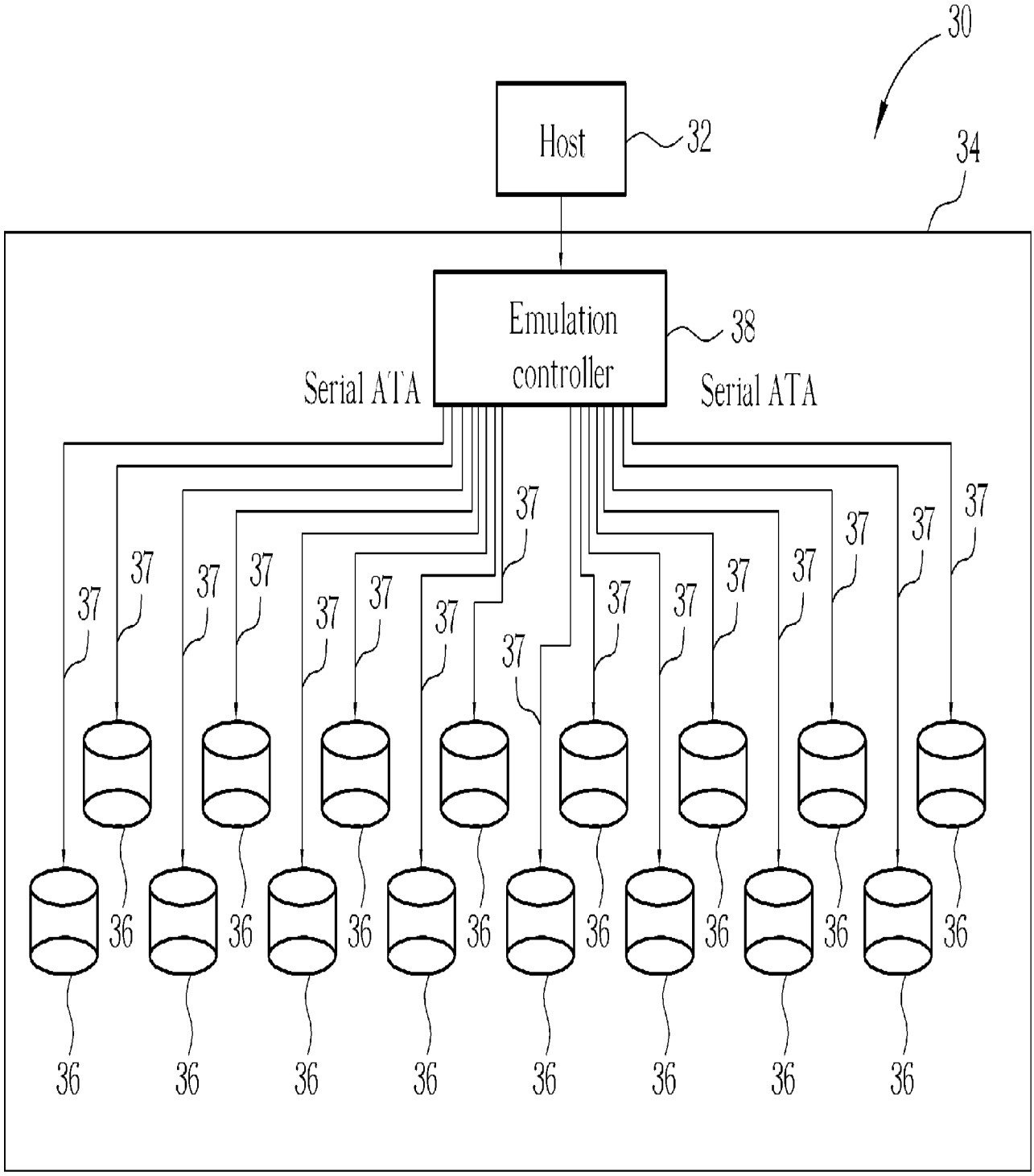
30
Host
32
34
Emulation controller
38
Serial ATA
Serial ATA
37
36

Fig. 3

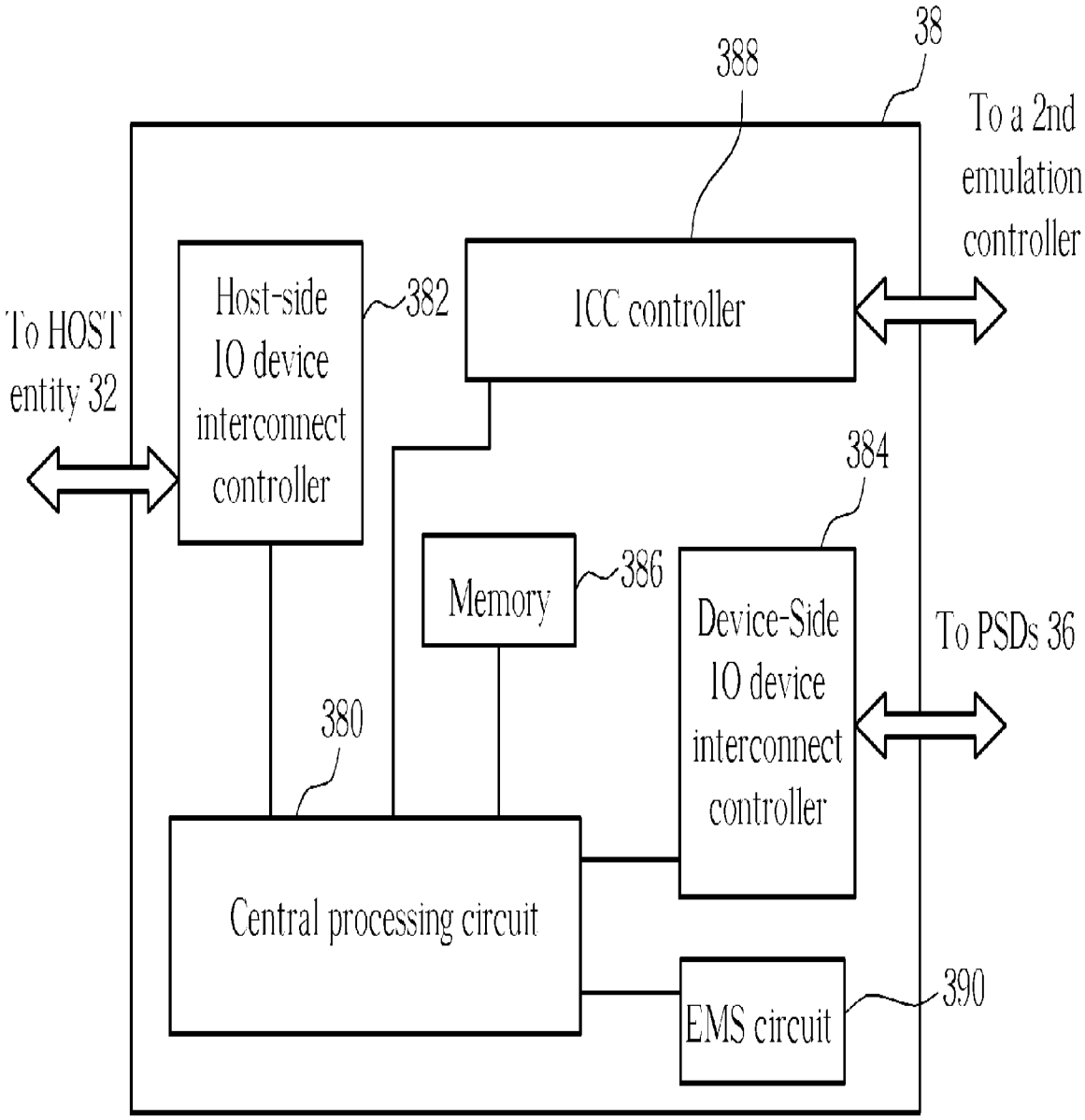
38
388
To a 2nd emulation controller
Host-side IO device interconnect controller
382
ICC controller
To HOST entity 32
384
Memory
386
Device-Side IO device interconnect controller
To PSDs 36
380
Central processing circuit
EMS circuit
390

Fig. 4

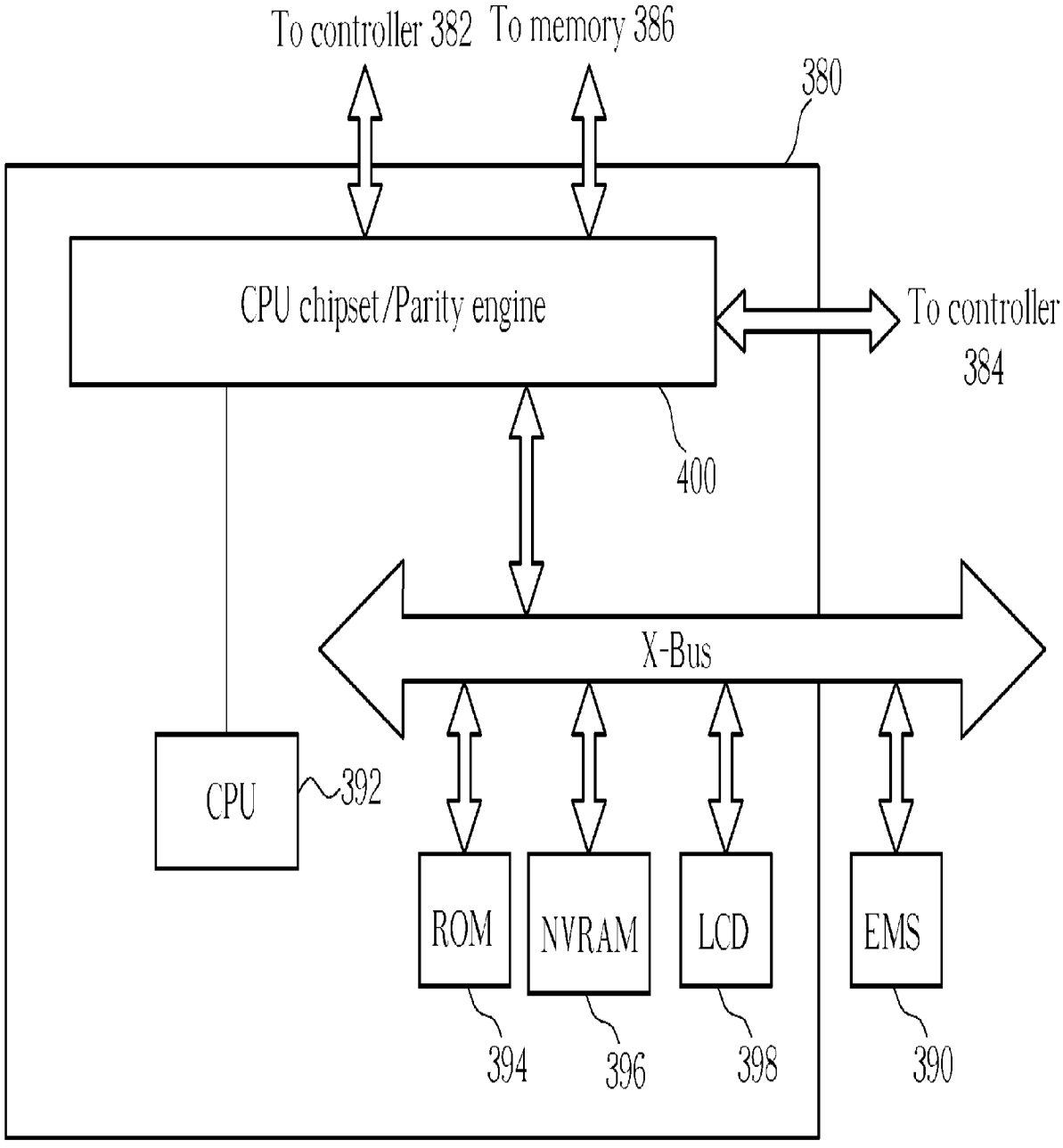
To controller 382
To memory 386
380
CPU chipset/Parity engine
To controller 384
400
X-Bus
CPU
392
ROM
NVRAM
LCD
EMS
394
396
398
390

Fig. 5

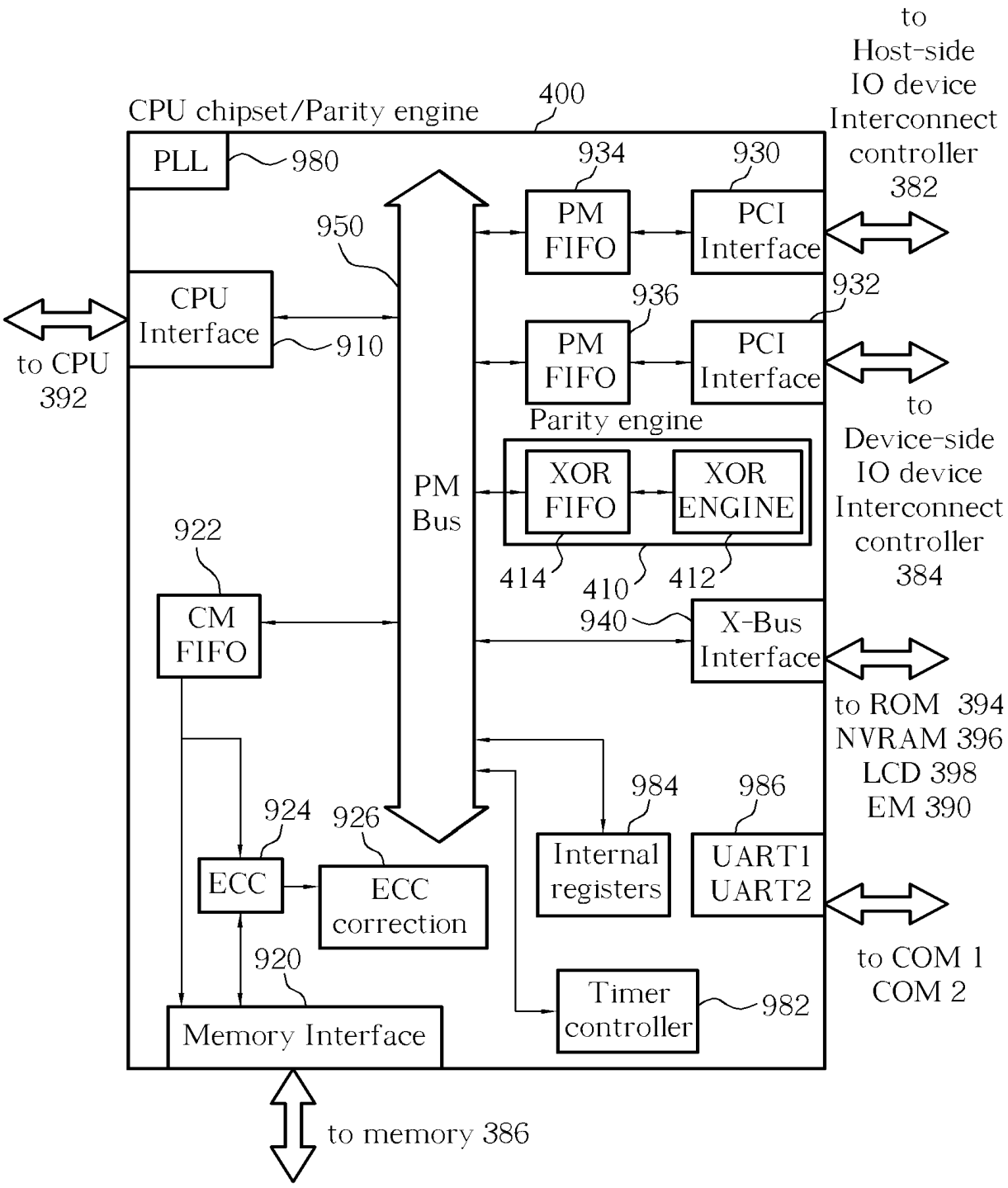
CPU chipset/Parity engine
400
PLL
980
950
934
930
PM FIFO
PCI Interface
to Host-side IO device Interconnect controller 382
CPU Interface
910
936
932
PM FIFO
PCI Interface
to CPU 392
Parity engine
to Device-side IO device Interconnect controller 384
PM Bus
XOR FIFO
XOR ENGINE
414
410
412
922
CM FIFO
940
X-Bus Interface
to ROM 394 NVRAM 396 LCD 398 EM 390
924
926
984
986
ECC
ECC correction
Internal registers
UART1 UART2
to COM 1 COM 2
920
Timer controller
982
Memory Interface
to memory 386

Fig. 6

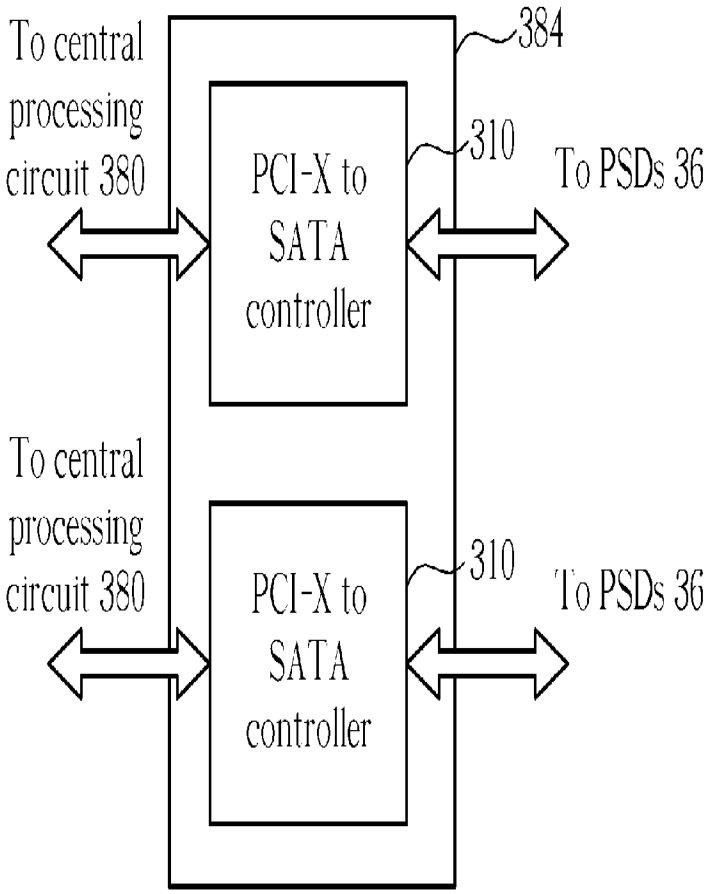
To central processing circuit 380
384
310
PCI-X to SATA controller
To PSDs 36
To central processing circuit 380
310
PCI-X to SATA controller
To PSDs 36

Fig. 7

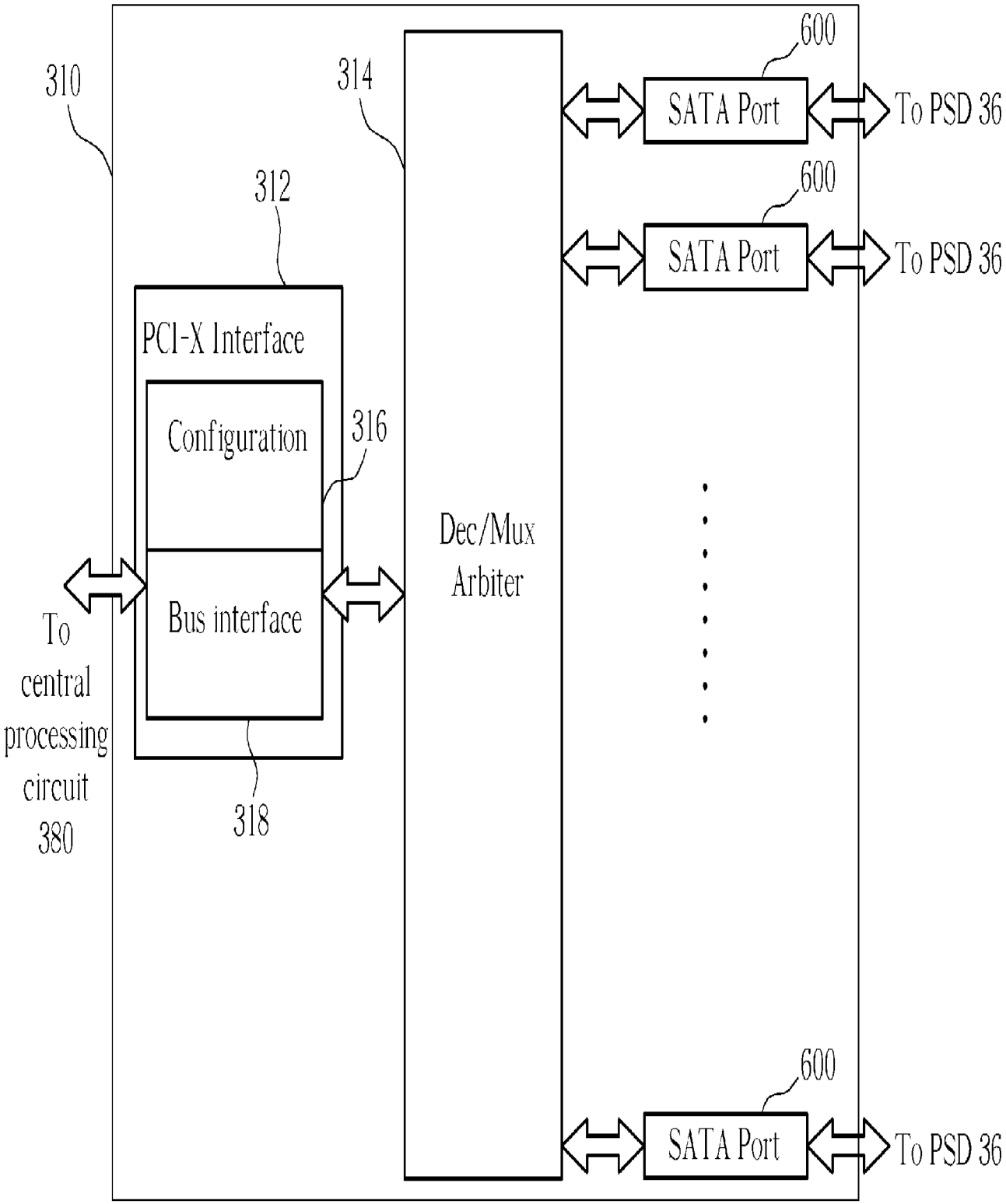
310
314
600
SATA Port
To PSD 36
312
600
SATA Port
To PSD 36
PCI-X Interface
Configuration
316
Dec/Mux
Arbiter
Bus interface
To
central
processing
circuit
380
318
600
SATA Port
To PSD 36

Fig. 8

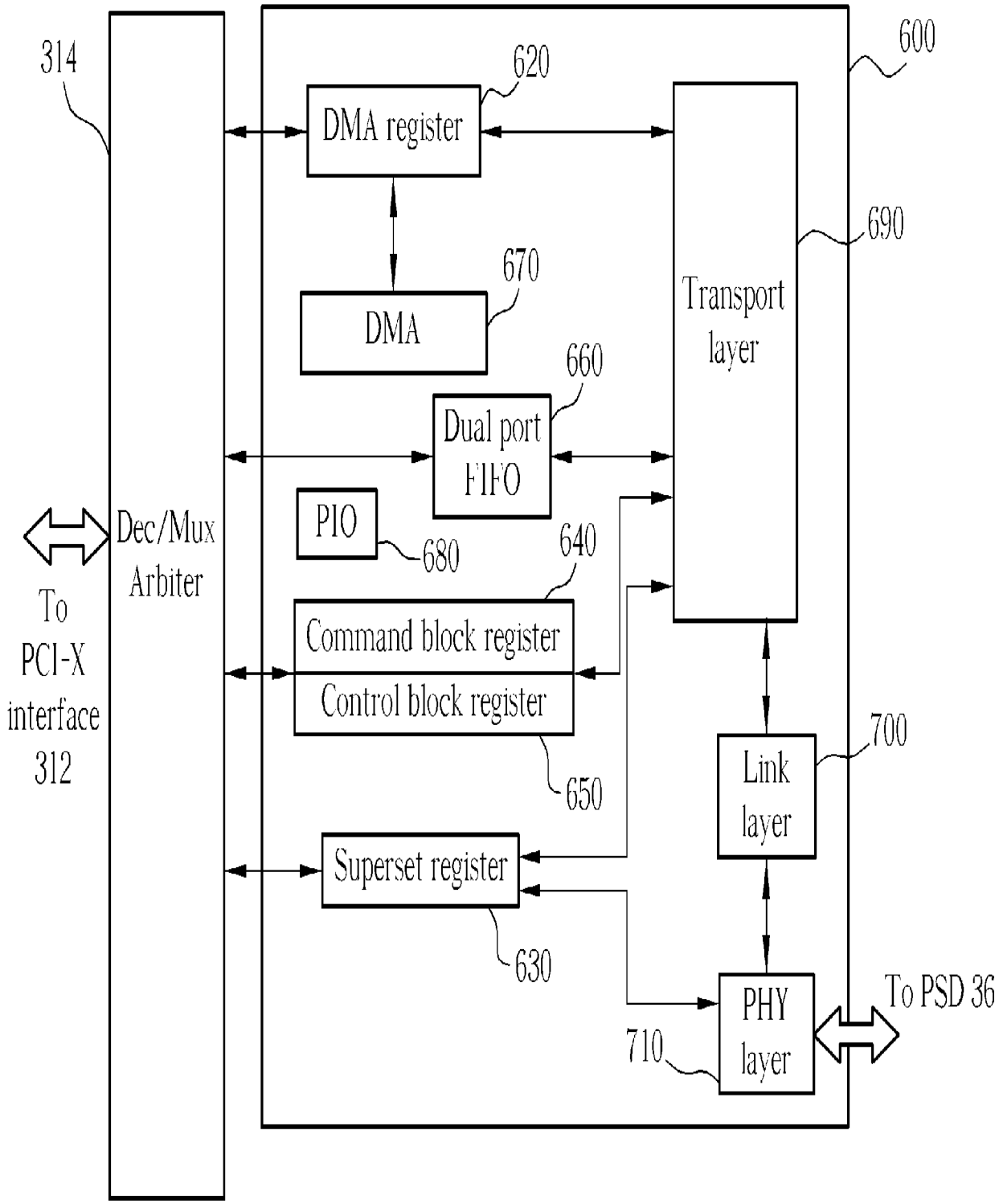
314
620
600
DMA register
690
670
DMA
Transport layer
660
Dual port FIFO
PIO
680
640
Dec/Mux Arbiter
To PCI-X interface 312
Command block register
Control block register
650
700
Link layer
Superset register
630
PHY layer
710
To PSD 36

Fig. 9

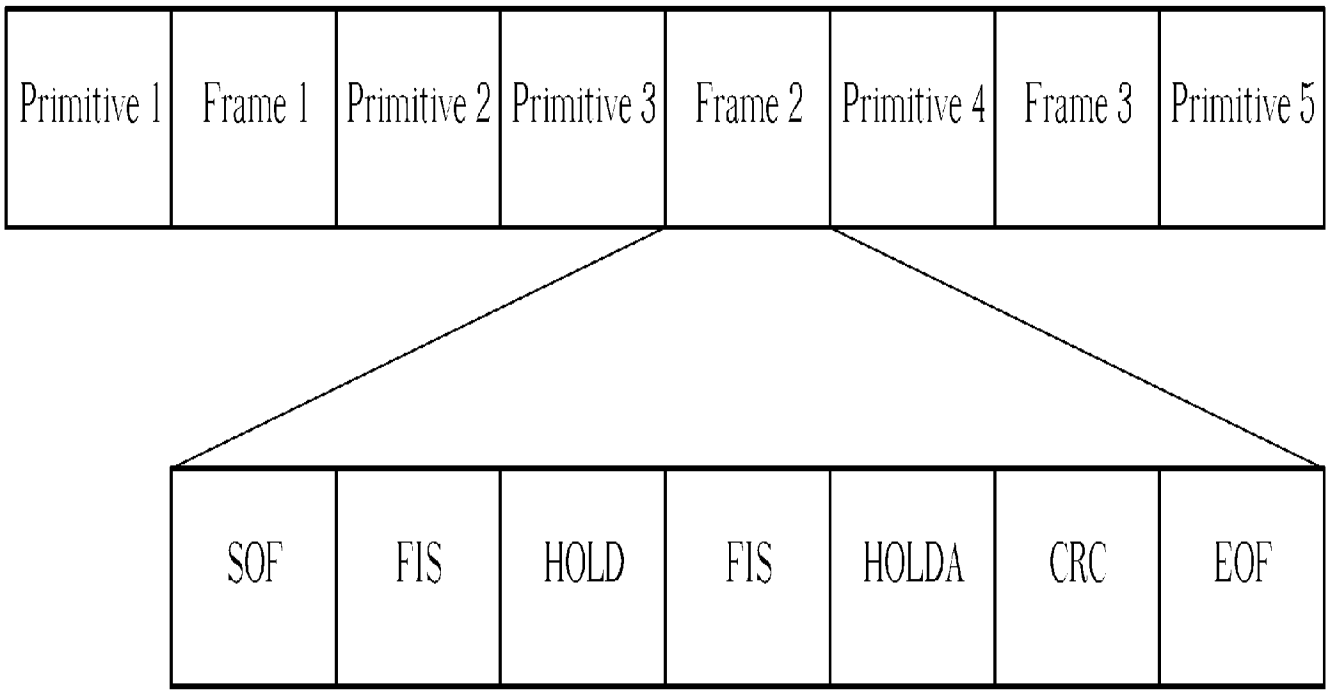
Primitive 1
Frame 1
Primitive 2
Primitive 3
Frame 2
Primitive 4
Frame 3
Primitive 5
SOF
FIS
HOLD
FIS
HOLDA
CRC
EOF

Fig. 10

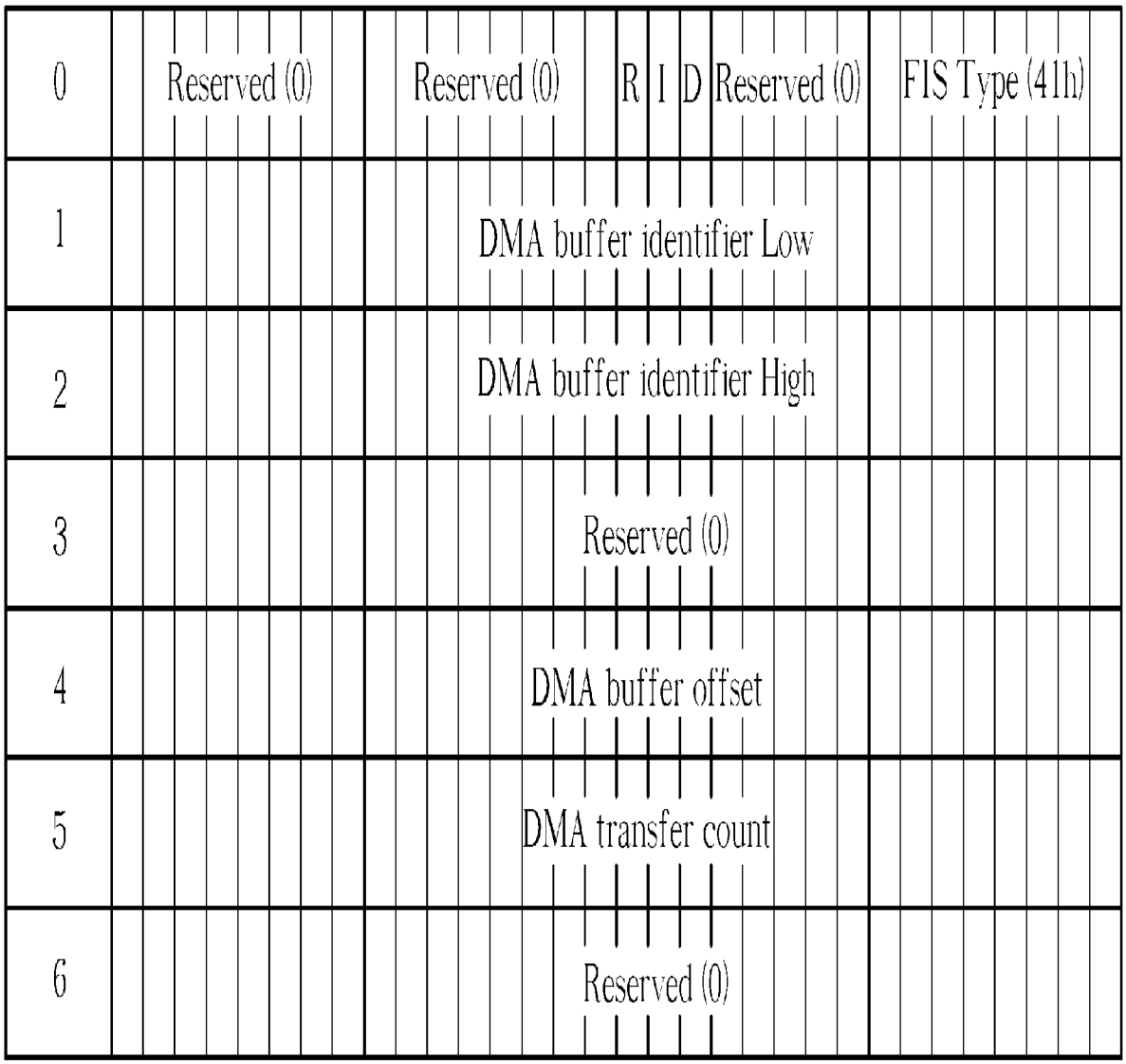
0
Reserved (0)
Reserved (0)
R
I
D
Reserved (0)
FIS Type (41h)
1
DMA buffer identifier Low
2
DMA buffer identifier High
3
Reserved (0)
4
DMA buffer offset
5
DMA transfer count
6
Reserved (0)

Fig. 11

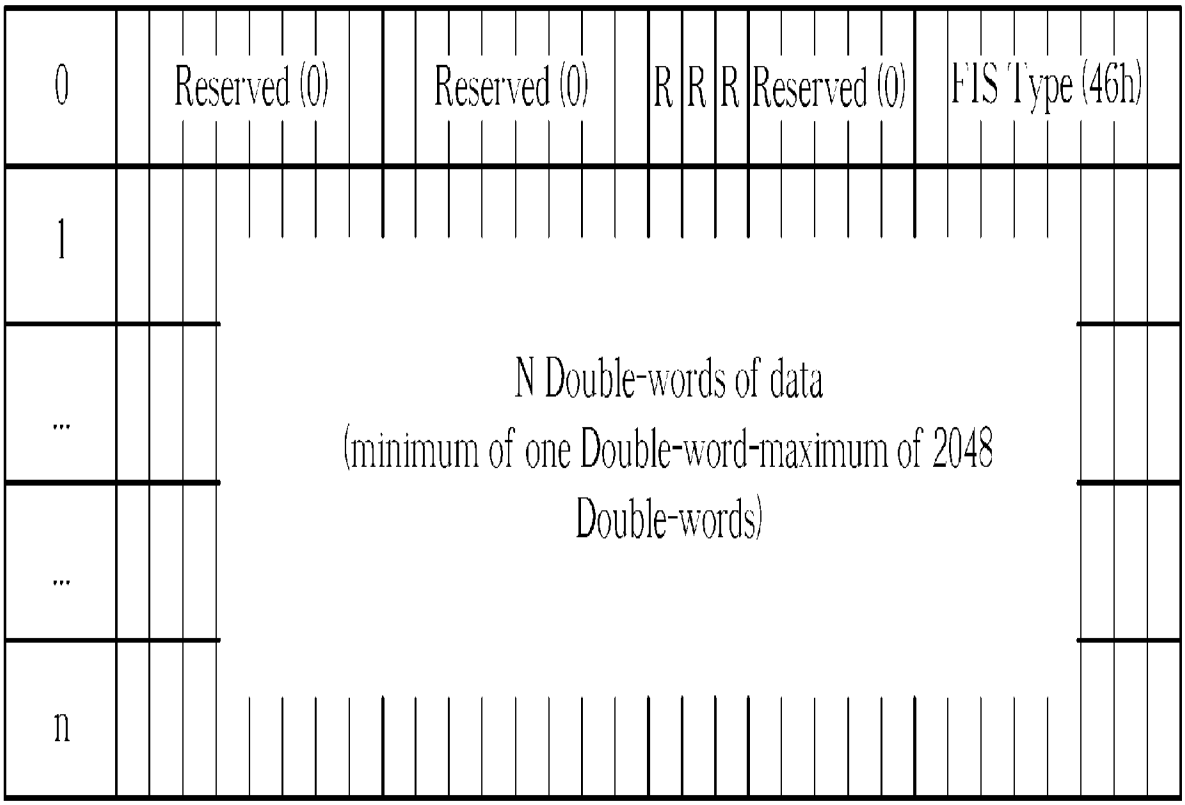
0
Reserved (0)
Reserved (0)
R R R
Reserved (0)
FIS Type (46h)
1
N Double-words of data
(minimum of one Double-word-maximum of 2048
Double-words)
...
...
n

Fig. 12

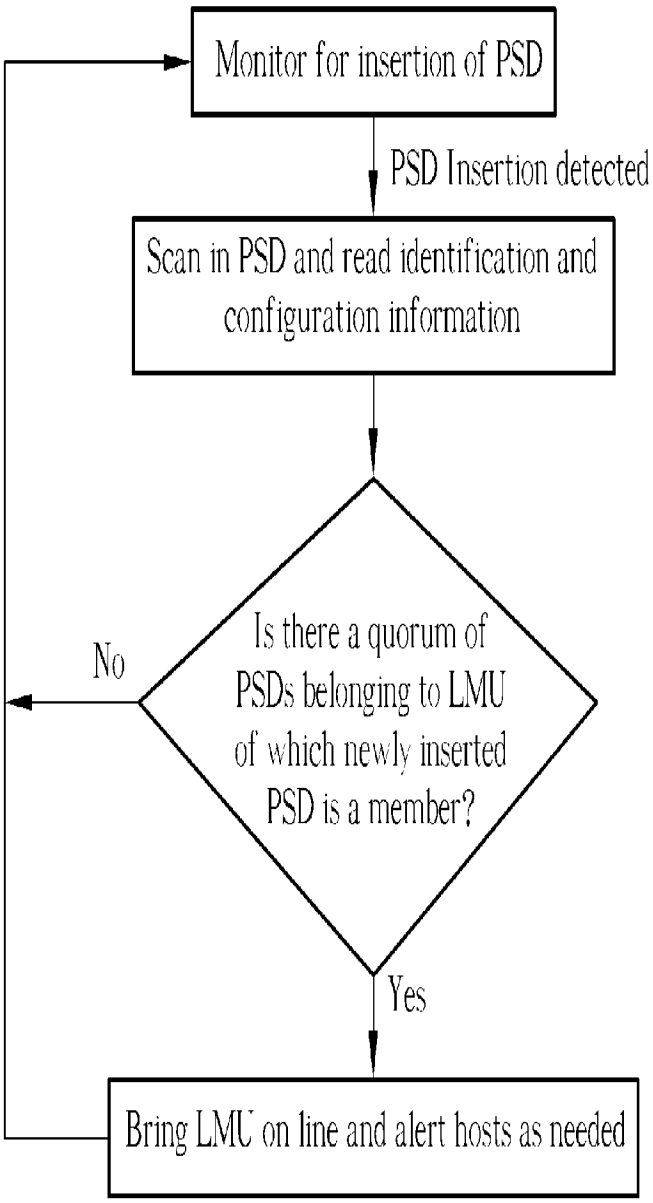
Monitor for insertion of PSD
PSD Insertion detected
Scan in PSD and read identification and configuration information
Is there a quorum of PSDs belonging to LMU of which newly inserted PSD is a member?
No
Yes
Bring LMU on line and alert hosts as needed

Fig. 13

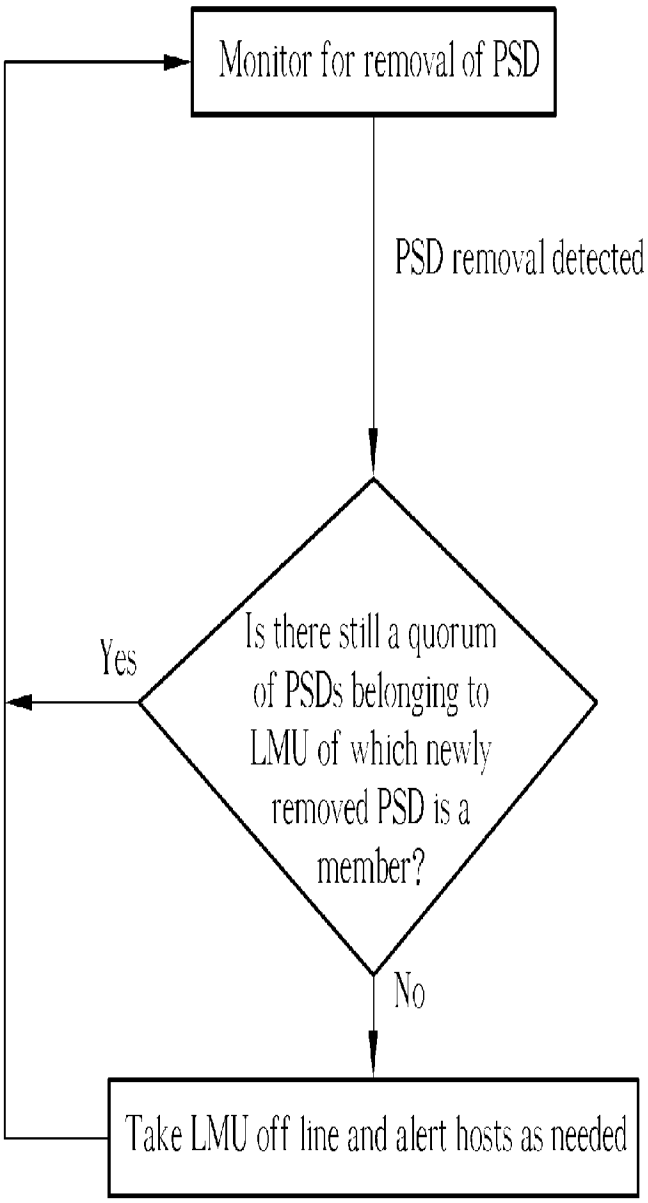
Monitor for removal of PSD
PSD removal detected
Is there still a quorum of PSDs belonging to LMU of which newly removed PSD is a member?
Yes
No
Take LMU off line and alert hosts as needed

Fig. 14

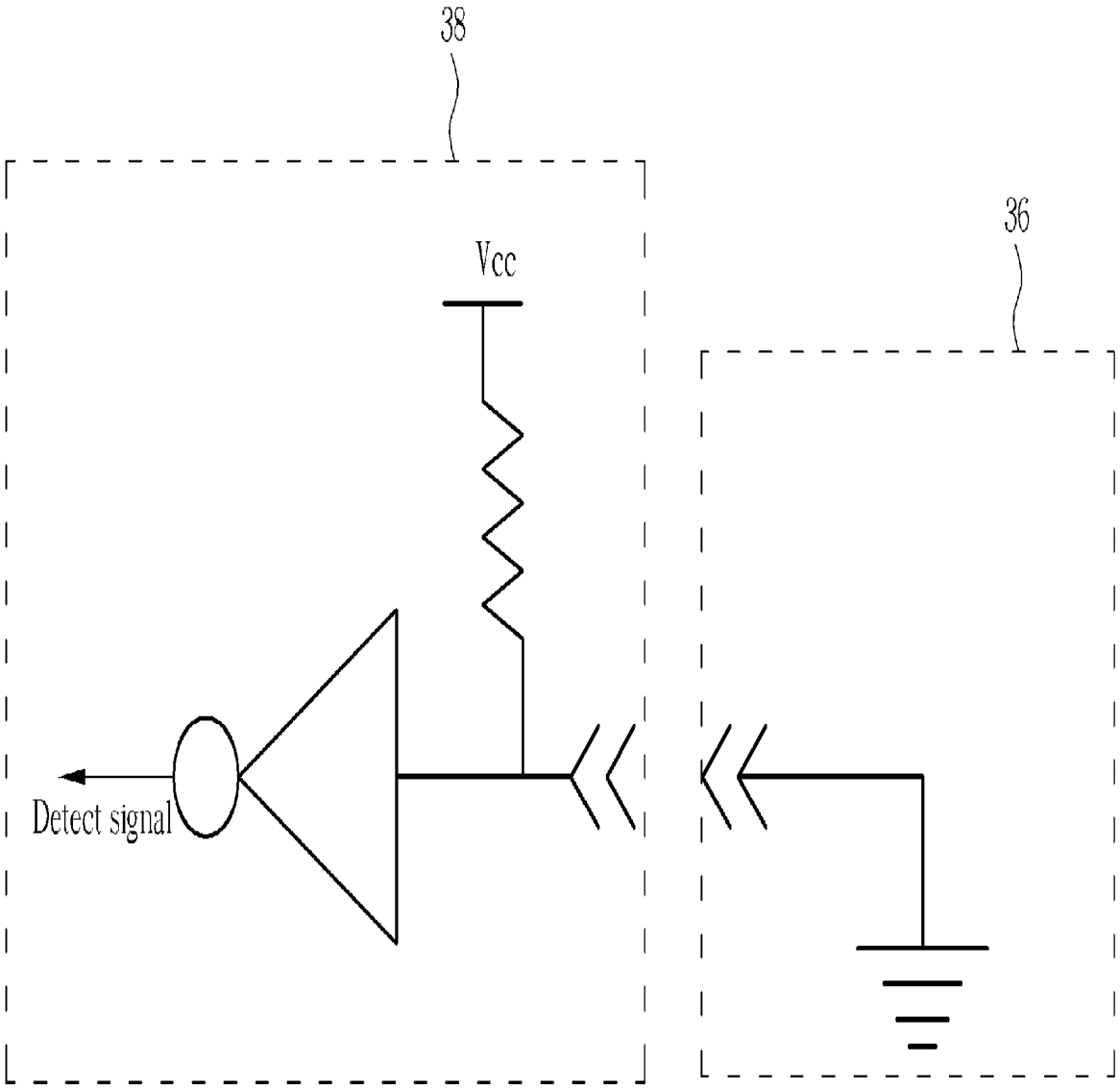

Fig. 15

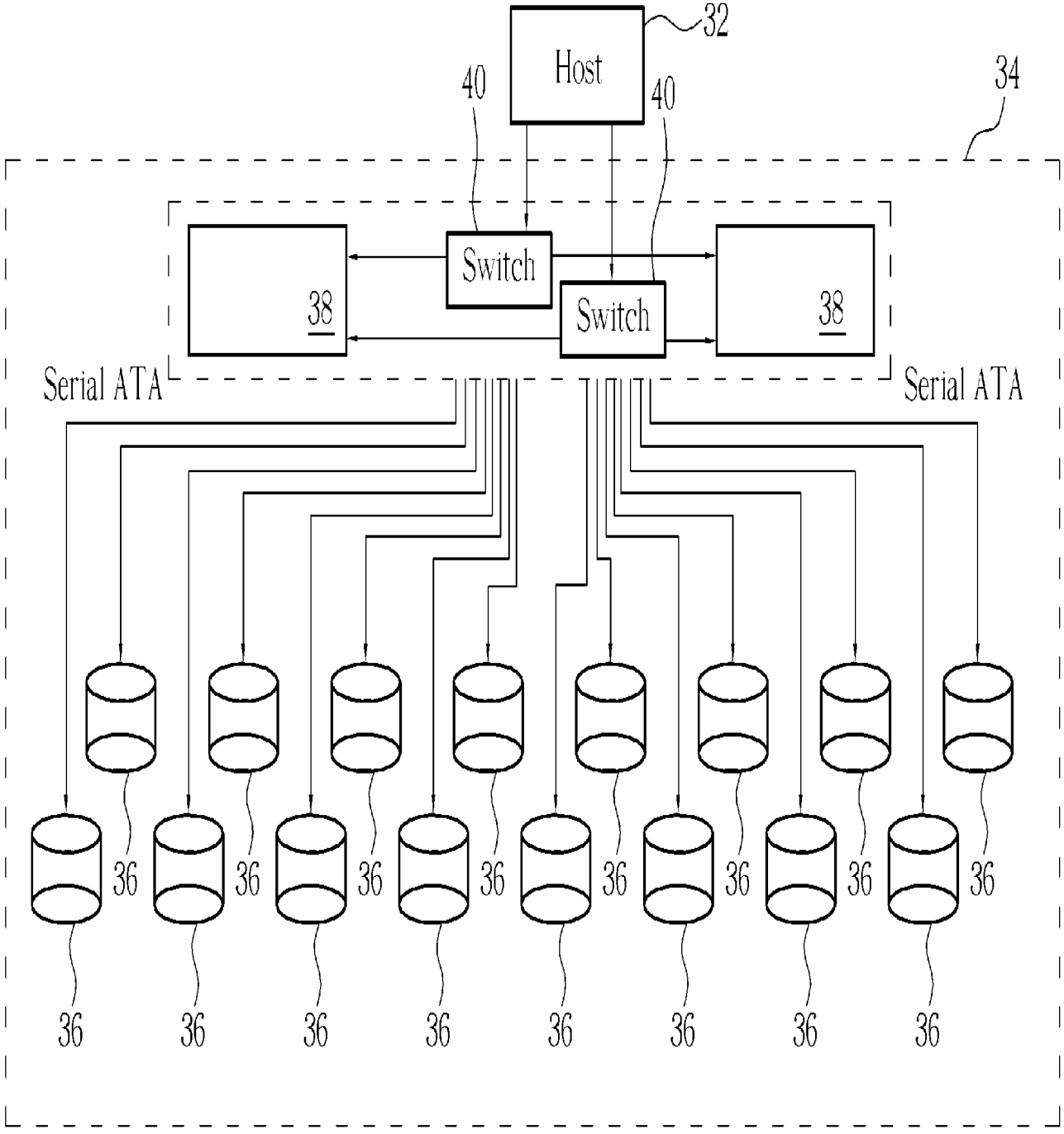

Fig. 16

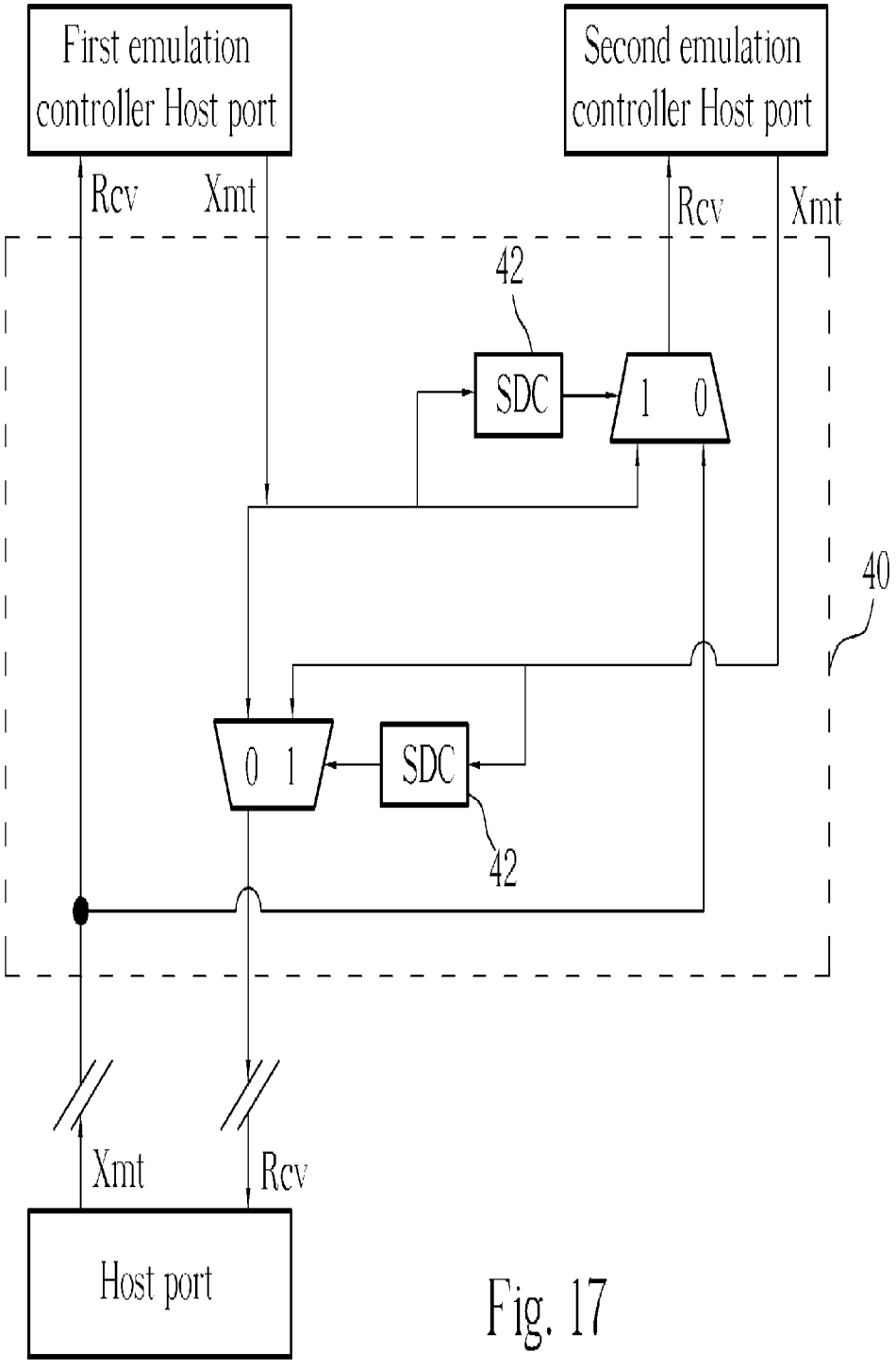
First emulation controller Host port
Second emulation controller Host port
Rcv
Xmt
Rcv
Xmt
42
SDC
1 0
40
0 1
SDC
42
Xmt
Rcv
Host port

Fig. 17

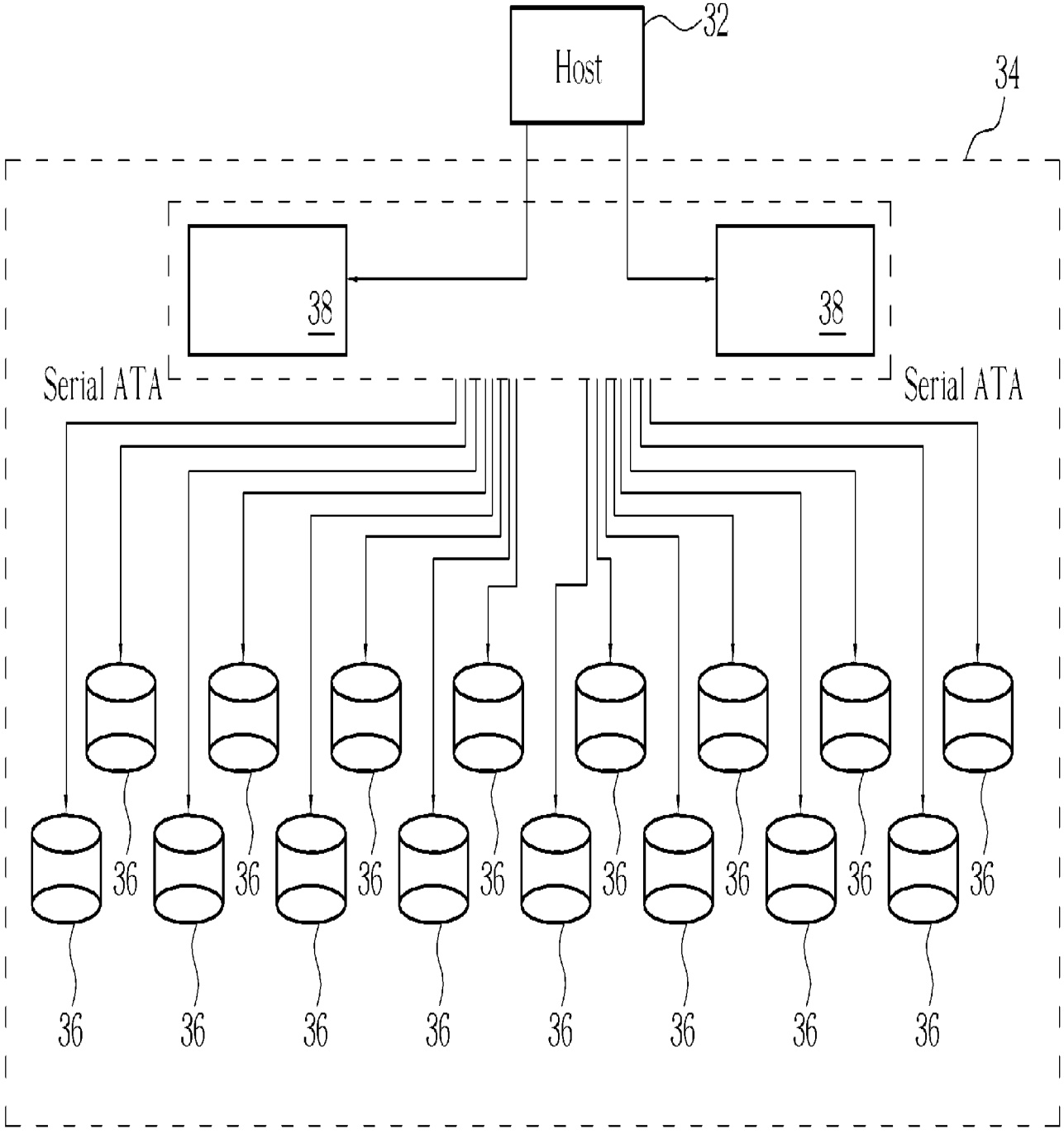

Fig. 18